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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,784	08/27/2003	Toru Mori	OKI.570	4482

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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,784	MORI ET AL.	
	Examiner	Art Unit	
	TAN N. TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 11/10/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *6,8 and 9* is/are rejected.

7)☒ Claim(s) *7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 6,8,9 is withdrawn in view of the reconsideration to claims 6,8,9. Rejections still based on the old cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6,8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Numata et al. (6,043,536).

With regard to claim 6, Numata et al. discloses a device comprising an SOI substrate having a SOI layer 7 including a region (CR) to which a first voltage is applied and an interface region (IR) to which a second voltage is applied; a device separation region 12 for separating the SOI layer 7 into the region (CR) and the interface region (IR) wherein a thickness of the SOI layer 7 of the region (CR) is thinner than a thickness of the SOI layer 7 of the interface region (IR), a plurality of first transistors 1B formed in the region (CR) and in which the SOI layer 7 of the above region (CR) is a fully depleted Si channel; and a plurality of second transistors 1A formed in the interface region (IR) and in which the SOI layer 7 of the above interface region is a fully depleted Si channel. (Note previous attachment #1, lines 41,42, column 8; lines 30-33, column 21, fig. 35 of Numata et al.). It is inherent that Numata et al. discloses a second driving voltage of an interface region is higher than the first driving voltage of the region (CR) because

the structure of Numata et al. is formed the same as that of applicant, thus the structure of Numata et al. has the same function as the applicant claimed invention. Numata et al. disclose all the claimed subject matter except for the region (CR) is to be a high speed computing region. However, it would have been obvious to one of ordinary skill in the art to recognize that the region (CR) of Numata et al. is a high speed computing region because it is conventional in the art to use a MOSFET for forming an LSI device in order to achieve reduction of consumption power and high speed circuit device. Note, lines 9-12, page 1 of background of the invention of applicant's invention, are cited to support for the well know position. Moreover, in reference to the claim language referring to the function of the region, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

With regard to claim 8, Numata et al. discloses a thickness of the SOI layer 7 of the above region (CR) is 20 nm. (Note previous attachment #1, lines 40,41, column 21, fig. 35 of Numata et al.).

With regard to claim 9, Numata et al. discloses a thickness of the SOI layer 7 of the interface region (IR) is 1 nm to 0.1 micrometer. (Note previous attachment #1, lines 38,39, column 21, fig. 35 of Numata et al.).

Allowable Subject Matter

3. Claims 7,10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7,10 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as a channel length of the first MOSFET formed in the high speed computing region is made shorter than a channel length of the second MOSFET formed in the interface region as recited in claim 7, and the first driving voltage is 1.5v and the second driving voltage is 3.3v as recited in claim 10.

4. Claims 1-4 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as the first driving voltage is 1.5v and the second driving voltage is 3.3v as recited in claim 1, and a channel length of the first MOSFET formed in the high speed computing region is made shorter than a channel length of the second MOSFET formed in the interface region as recited in claim 2.

Response to Arguments

5. Applicant's arguments filed 3/22/05 have been fully considered but they are not persuasive.

It is argued, at page 10 of the remarks, that "the prior art as replied upon by the examiner does not disclose an LSI device including an SOI substrate having a high speed computing region and an interface region, does not respective first and second driving voltages for a high speed computing region and an interface region and does not disclose a second driving voltage that is higher than a first driving voltage". However, the previous attachment #1, lines 41,42, column 8; lines 30-33, column 21, fig. 35 of Numata et al. do show a device comprising an SOI substrate having a SOI layer 7 including a region (CR) to which a first voltage is applied and an interface region (IR) to which a second voltage is applied. It is inherent that Numata et al. discloses a second driving voltage of an interface region is higher than the first driving voltage of the region (CR) because the structure of Numata et al. is formed the same as that of applicant, thus the structure of Numata et al. has the same function as the applicant claimed invention. Numata et al. disclose all the claimed subject matter except for the region (CR) is to be a high speed computing region. However, it would have been obvious to one of ordinary skill in the art to recognize that the region (CR) of Numata et al. is a high speed computing region because it is conventional in the art to use a MOSFET for forming an LSI device in order to achieve reduction of consumption power and high speed circuit device. Note, lines 9-12, page 1 of background of the invention of applicant's invention, are cited to support for the well know position. Moreover, in reference to the claim language referring to the function of the region, intended use and other types of functional language must result in a structural difference between the claimed invention

and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). In addition, the term "high speed" recited in claim 6 does not clearly set forth the metes and bounds of the patent protection desired. Note In re Hammack 166 USQ 240 (CCPA 1970) and In re Moore, 169 USPQ 236 (CCPA 1971), claims must be analyzed to determined their metes and bounds so that, it is clear from the claim language what subject matter the claims encompass. Further, applicant's claim 6 does not recite the interface region is an I/O region, therefore applicant's claims 6,8,9 do not distinguish over Numata et al. reference.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (571) 272-1923. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TT

Nov 2005